Influence of Jitter on Limit Cycles in Bang-Bang Clock and Data Recovery Circuits

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***Abstract*——In bang-bang (BB) clock and data recovery circuits (CDR) limit cycles can occur, but these limit cycles are undesired for a good operation of the BB-CDR. Surprisingly, however, a little bit of noise in the system is beneficial, because it will quench the limit cycles. Until now, authors have always assumed that there is enough noise in a BB-CDR such that no limit cycle occurs. In this work, a pseudo-linear analysis based on describing functions is used to investigate this. In particular, the relationship between the input noise and the amplitude of eventual limit cycles is investigated. An important result of the theory is that it allows to quantify the influence of the different loop parameters on the minimal amount of input jitter needed to destroy the limit cycle. Additionally, for the case that there is not enough noise, the worst case amplitude of the limit cycle (which is unavoidable in this case) is quantified as well. The presented analysis exhibits excellent matching with time domain simulations and leads to very simple analytical expressions.**

Keywords—Bang-bang (BB) phase detector (PD), Charge pump (CP) clock and data recovery (CDR), describing functions, jitter, limit cycle, modeling.

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